Problem Report PR-012

HW part: HW0001

HW rev: R002

SW rev: 2021-07-29

Test log: 20210729-Piano session

Description: The data looks OK on the logic analyzer, but the synthesizer doesn’t see the data.

Steps to reproduce the problem

1. Start test software
2. Play piano
3. Observe no activity on the synthesizer
4. Turn piano off
5. Observe active sense warning message

Investigation notes

2021-07-29: After observing that the desired design wouldn’t fit in the device, I decided to implement the FPGA as a SPI to UART bridge, with no buffering. With no synchronization, I needed to add some delay in the microcontroller code so it didn’t miss data (on the logic analyzer). However, I noticed when I connected this to the synthesizer, it did not read any of the data. I’ll probably need to include buffering between the SPI output and the UART input in the FPGA.